19-1866; Rev 0; 12/00

MAXIM

MAX3950 Evaluation Kit

Evaluates: MAX3950

General Description

The MAX3950 evaluation kit (EV kit) is an assembled surface-mount demonstration board that provides easy evaluation of the MAX3950 10Gbps, 1:16 deserializer with low-voltage differential signal (LVDS) outputs. All components necessary to interface with 3.3V CML inputs and LVDS outputs are included on the EV kit.

Features

- **+3.3V Single Supply**
- **9.95Gbps/10.7Gbps Evaluation**
- **Fully Assembled and Tested Surface-Mount Board**

Component List

DESIGNATION	QTY	DESCRIPTION
C1, C10–C13	5	1000pF ±10% ceramic capacitors (0402) Murata GRM36X7R102K050A
C2, C6–C9, C14–C17	9	0.01µF ±10% ceramic capacitors (0402) Murata GRM36X7R103K016A
C3	1	33µF ±10%, 10V min tantalum capacitor, AVX TAJC336K035
C4	1	2.2µF ±10%, 16V min tantalum capacitor, AVX TAJC225K016
C5	1	0.1µF ±10% ceramic capacitor (0603) Murata GRM39X7R104K016A
J1, J2, J7–J38	34	SMB connectors (PC mount)
J3–J6	4	SMA connectors (edge mount)
J39, J40	2	Test points
J41–J46	6	Not installed
J47	1	2 ×10 header (0.1in center)
L1	1	56nH inductor Coilcraft 0805HS-560TKBC
R1–R17	17	Not installed
U1	1	MAX3950EGK 68-pin QFN
None	1	MAX3950 EV kit circuit board
None	1	MAX3950 data sheet
None	1	MAX3950 EV kit data sheet

Ordering Information

PART	TEMP. RANGE	IC-PACKAGE
MAX3950EVKIT	-40°C to +85°C	68 QFN

Component Suppliers

SUPPLIER	PHONE	FAX
AVX	843-448-9411	843-626-3123
Murata	770-684-7821	—

Note: *Please indicate that you are using the MAX3950 when contacting the suppliers.*

Detailed Description

The MAX3950 EV kit simplifies evaluation of the MAX3950 1:16 deserializer. The EV kit operates from a single +3.3V supply and includes all the external components necessary to interface with 3.3V CML inputs and LVDS outputs. Transmission line test structures are included on the evaluation board to allow for measurement of signal loss and dispersion of clock and data signals at 10GHz.

Applications information

Connecting LVDS Outputs to 50Ω Oscilloscope Inputs

To monitor LVDS signals with 50Ω oscilloscope inputs, set the inputs of the oscilloscope to "AC coupling" or place a DC block in series with each output. If you are observing only one output with a 50Ω probe, balance the complementary output with a DC block and a 50Ω terminator to ground.

Connecting LVDS Outputs to High-Impedance Oscilloscope Inputs

To monitor LVDS signals with high-impedance oscilloscope inputs, install 100Ω 0402 resistors on locations R1 through R17. Note that this does not provide as good a termination scheme as using the 50Ω inputs on an oscilloscope and the resulting output will be degraded.

Exposed Pad Package

The 68-pin QFN package with exposed pad incorporates features that provide a very low thermal-resistance path for heat removal from the IC—either to a PC board or to an external heatsink. The MAX3950's exposed pad must be soldered directly to a ground plane with good thermal conductance.

Shunt Configuration of J47

The 2 × 10 header on J47 should be shunted as shown in Figure 1. Other jumper arrangements will cause the IC to operate erroneously.

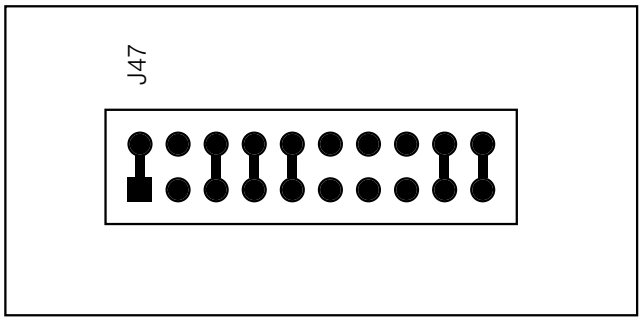

Figure 1. Shunt Arrangement for J47

Layout Consideration

The MAX3950's performance can be greatly affected by circuit-board layout and design. Use good high-frequency design techniques, including minimizing ground inductances and using fixed-impedance transmission lines on the data and clock signals.

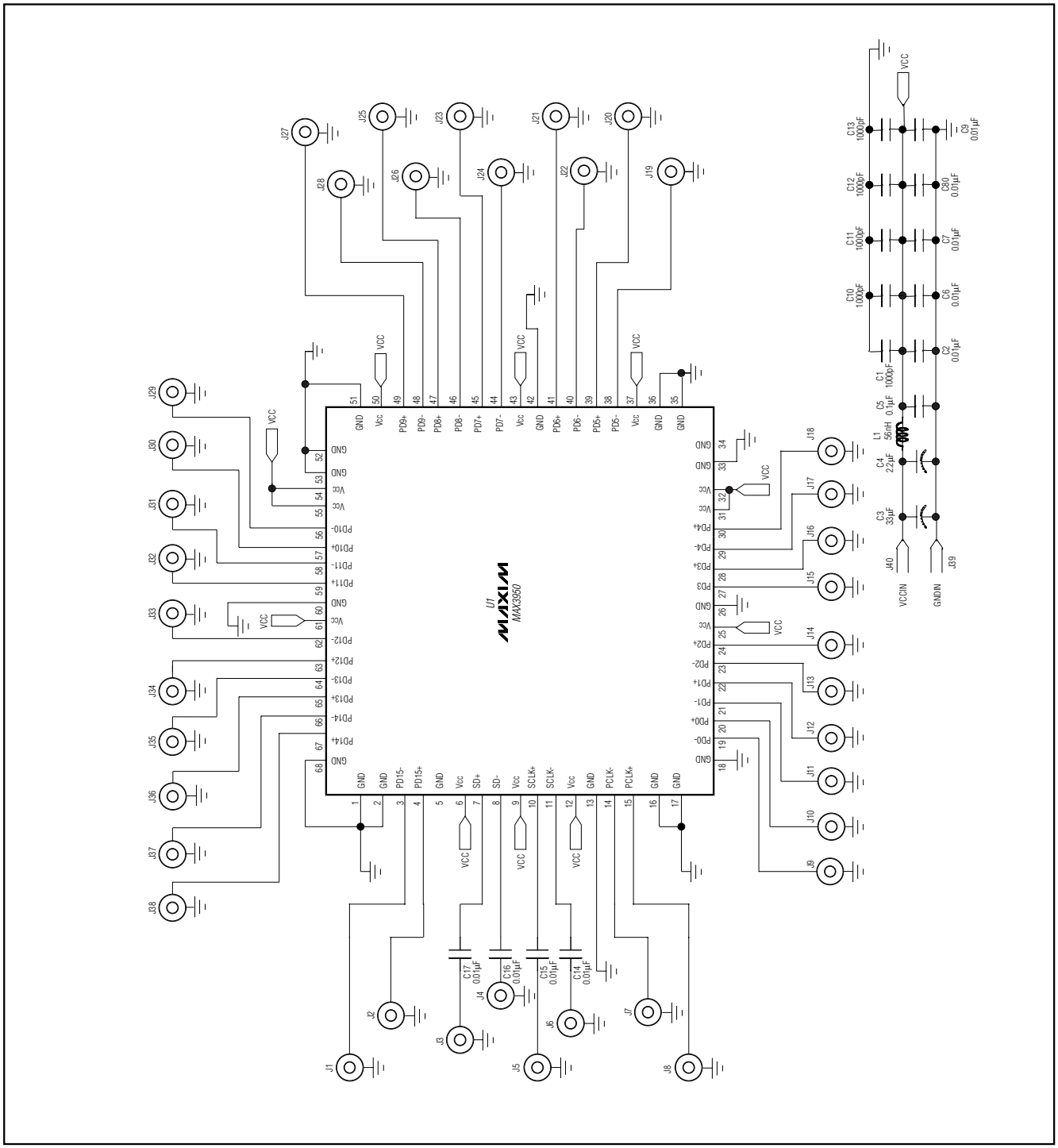

Figure 2. MAX3950 EV Kit Schematic

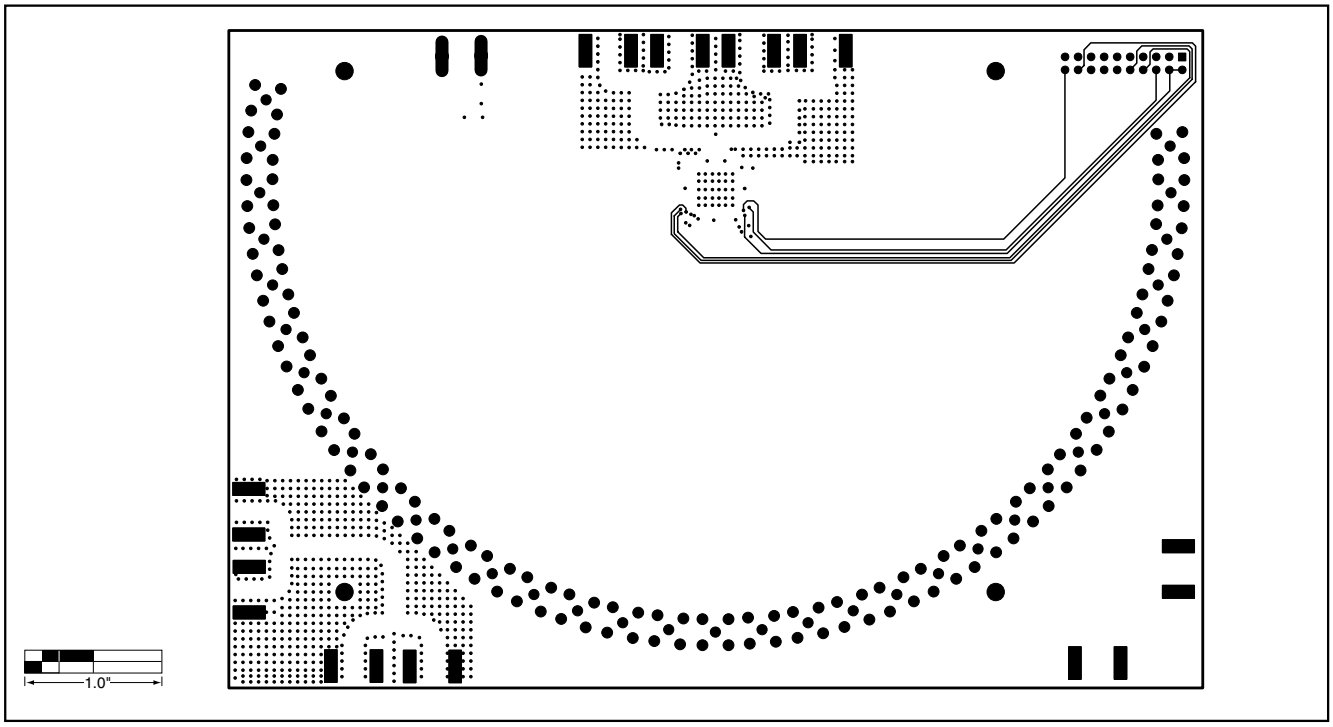

Figure 3. MAX3950 EV Kit PC Board Layout—Solder Side

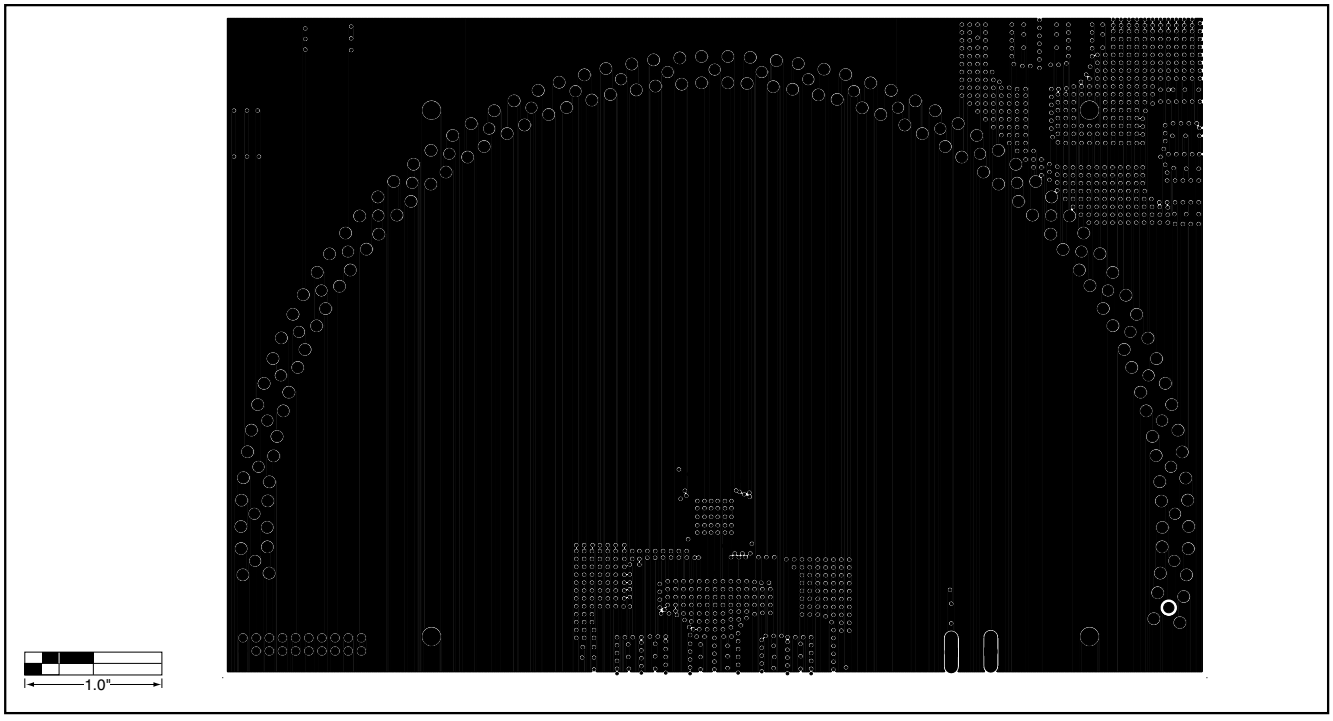

Figure 4. MAX3950 EV Kit PC Board Layout—Power Plane

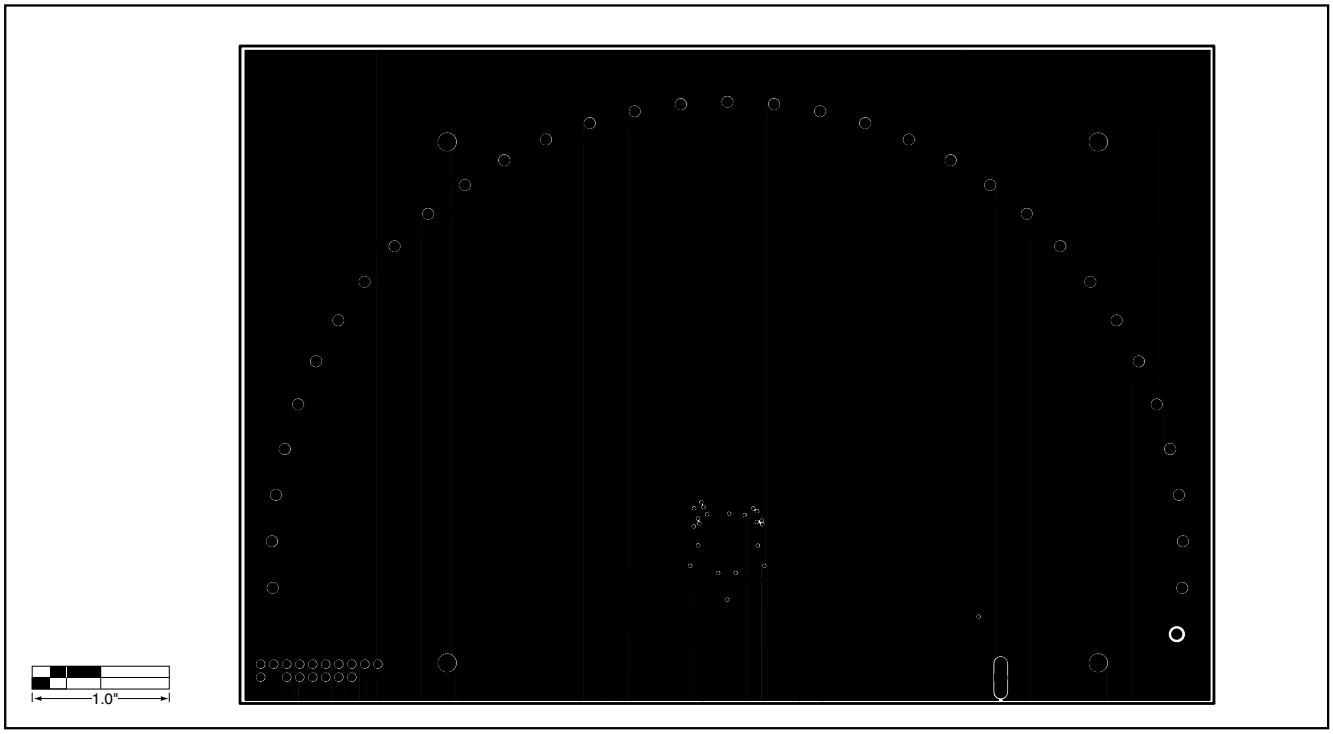

Figure 5. MAX3950 EV Kit PC Board Layout—Ground Plane

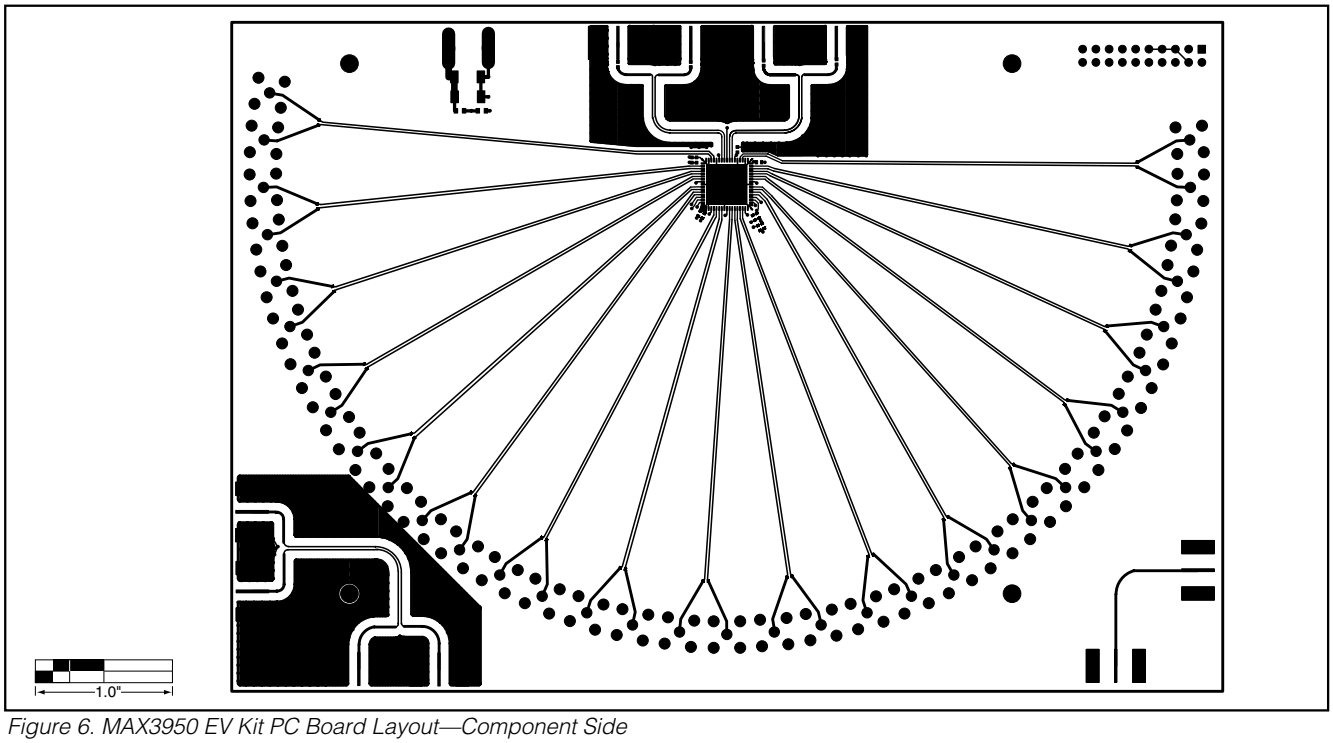

Figure 6. MAX3950 EV Kit PC Board Layout—Component Side

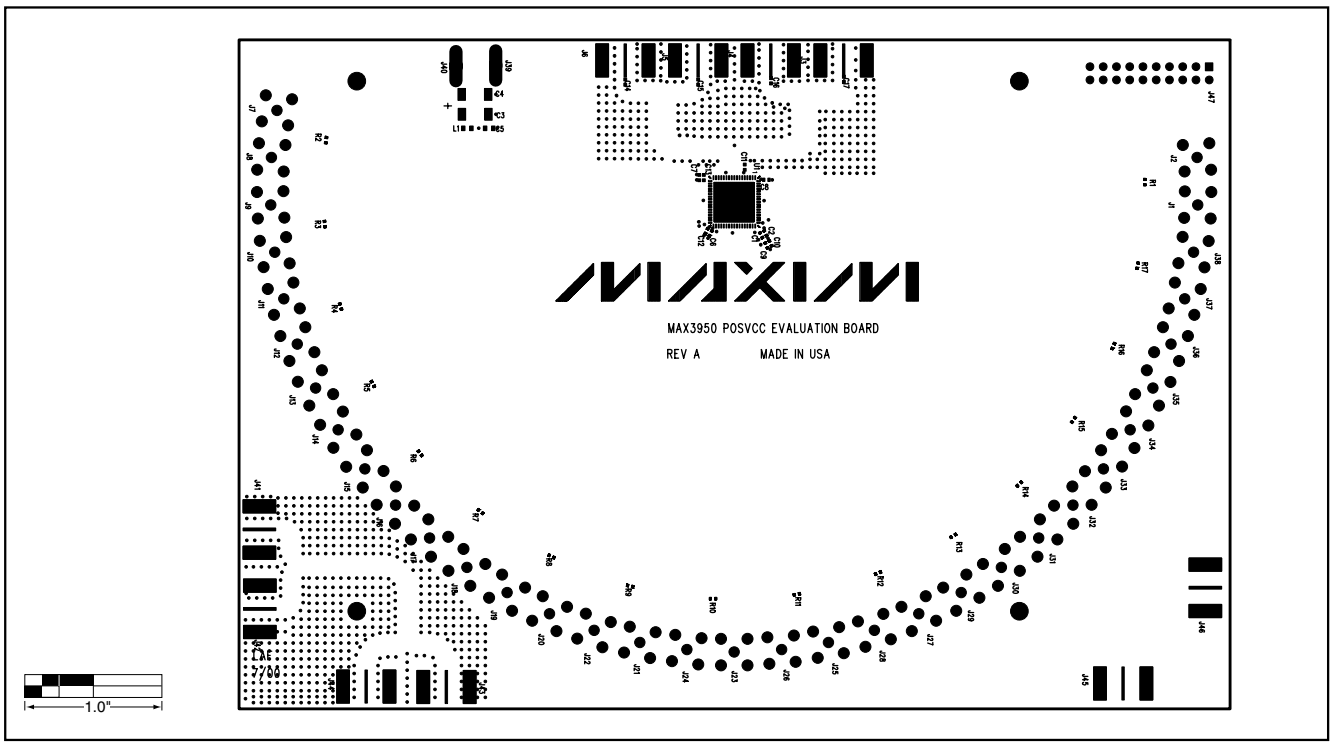

Figure 7. MAX3950 EV Kit Component Placement Guide—Component Side